What Is Claimed Is:

1. A self-aligned method of forming a semiconductor memory array of floating gate memory cells in a semiconductor substrate, each memory cell having a floating gate, a first terminal, a second terminal with a channel region therebetween, and a control gate, the method comprising the steps of:

a) forming a plurality of spaced apart isolation regions on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions, the active regions each comprising a first layer of insulation material on the semiconductor substrate and a first layer of conductive material on the first layer of insulation material;

b) forming a plurality of spaced apart first trenches across the active regions and isolation regions which are substantially parallel to one another and extend in a second direction that is substantially perpendicular to the first direction; each of the first trenches being substantially rectangularly shaped and exposing the first layer of the conductive material in each of the active regions;

c) forming a second layer of insulation material in each of the active regions that is disposed adjacent to and over the first layer of conductive material;

d) filling each of the first trenches with a second conductive material to form blocks of the second conductive material having a substantially rectangular shape, wherein for each of the active regions, each of the blocks is adjacent to the second layer of insulation material and is insulated from the substrate;

e) forming a sidewall spacer of a conductive material immediately adjacent to and contiguous with each of the blocks along the second direction, wherein for each active region each spacer is disposed over the second layer of insulation material and the first layer of conductive material;

f) forming a plurality of first terminals in the substrate, wherein in each of the active regions each of the first terminals is adjacent to one of the blocks; and

g) forming a plurality of second terminals in the substrate, wherein in each of the active regions each of the second terminals is spaced apart from the first terminals and is below the first layer of conductive material.

2. The method of claim 1, wherein the formation of the second layer of insulation material includes oxidizing top and side portions of the first layer of conductive material in each active region.

3. The method of claim 1, further comprising the steps of:

h) forming a plurality of spaced apart second trenches across the active regions and isolation regions which are substantially parallel to one another and extend in the second direction; each of the second trenches being formed between selected pairs of the blocks and extending through the first layer of conductive material and the first layer of insulation material to expose the second terminal;

i) forming a third layer of insulation material along sidewalls of the second trenches;

j) filling each of the second trenches with a conductive material that is insulated from the first conductive layer by the third layer of insulation material.

4. The method of claim 3, wherein the formation of the third layer of insulation material includes oxidizing end portions of the first layer of conductive material that face the second trenches.

5. The method of claim 3, wherein the formation of the third layer of insulation material includes forming a pair of inner sidewall spacers of an insulation material along sidewalls of each of the second trenches.

6. The method of claim 3, wherein the formation of the third layer of insulation material includes the steps of:

oxidizing end portions of the first layer of conductive material that face the second trenches; and

forming a pair of inner sidewall spacers of an insulation material along sidewalls of each of the second trenches.

7. The method of claim 1, wherein each of the blocks and corresponding spacer formed contiguously therewith form a control gate having a notch at the connection between the block and the spacer.

8. The method of claim 1, further comprising the step of forming a layer of metalized silicon on each of the blocks of second conductive material.

9. The method of claim 1, wherein the formation of the first trenches comprises the steps of:

forming at least one layer of material over the first layer of conductive material,

selectively etching through the at least one layer of material to form top portions of the first trenches;

forming a pair of sidewall spacers on side walls of each of the first trenches;

etching between each pair of the sidewall spacers of each of the first trenches and through the first layer of conductive material to form bottom portions of the first trenches;

wherein the bottom portions of the first trenches have a smaller width than that of the top portions of the first trenches.

10. The method of claim 1, wherein at least a portion of the second layer of insulation material is formed by forming a layer of insulation material along entire sidewalls of the first trenches.

11. The method of claim 1, wherein at least part of the second layer of insulation material is formed by forming a layer of insulation material on an upper surface of the first layer of conductive material.

12. The method of claim 1, wherein:

the formation of the first trenches includes the formation of intermediate trenches between selected pairs of the first trenches across the active regions and isolation regions, the intermediate trenches are substantially parallel to one another and extend in the second direction; and

the filling of the first trenches includes the filling of the intermediate trenches with the second conductive material to form blocks of the second conductive material in the intermediate trenches.

13. The method of claim 12, further comprising the step of forming a layer of metalized silicon on each of the blocks of second conductive material.

14. The method of claim 12, further comprising the steps of:

h) forming a plurality of spaced apart second trenches across the active regions and isolation regions which are substantially parallel to one another and extend in the second direction, the second trenches being formed by removing the second conductive material in the intermediate trenches, and extending the intermediate trenches through the first layer of conductive material and the first layer of insulation material to expose the second terminal;

i) forming a third layer of insulation material along sidewalls of the second trenches;

j) filling each of the second trenches with a conductive material that is insulated from the first conductive layer by the third layer of insulation material.

15. The method of claim 1, further comprising the steps of:

forming a second sidewall spacer of insulating material along a sidewall of each of the blocks of conductive material; and

forming a layer of metalized silicon on each of the first terminals immediately adjacent to one of the second sidewall spacers, wherein each of the layers of metalized silicon is self-aligned to the one of the second sidewall spacers.

16. The method of claim 1, further comprising the step of:

forming a layer of metalized silicon on each of the blocks of second conductive material, wherein for each of the first trenches, a sidewall of the first trench aligns an edge of the metalized silicon to an edge of the block of second conductive material.

17. The method of claim 1, further comprising the step of:

forming a third layer of insulation material over the layer of metalized silicon, wherein for each of the first trenches, a sidewall of the first trench aligns an edge of the third layer of insulation material to an edge of the block of second conductive material.

18. The method of claim 15, further comprising the step of:

forming a conductive material over each of the layers of metalized silicon and up against the second sidewall spacer self aligned thereto.

19. The method of claim 15, wherein the formation of each of the second sidewall spacers includes forming a layer of insulation material between the second sidewall spacer and the sidewall of the block of conductive material.

20. The method of claim 1, further comprising the steps of:

forming a second sidewall spacer of insulating material along a sidewall of each of the blocks of conductive material such that pairs of the second sidewall spacers are adjacent to but spaced apart from each other with one of the first terminals substantially therebetween;

forming a layer of metalized silicon on each one of the first terminals between a pair of the second sidewall spacers corresponding to the one first terminal such that the layer of metalized silicon is self-aligned to the one first terminal by the corresponding pair of second sidewall spacers;

forming a layer of passivation material over the active regions;

forming contact openings through the passivation material, wherein for each of the contact openings:

the contact opening extends down to and exposes one of the metalized silicon layers,

the contact opening has a lower portion bounded by the corresponding pair of second sidewall spacers, and

the contact opening has an upper portion that is wider than a spacing between the corresponding pair of second sidewall spacers; and

filling each of the contact openings with a conductive material.

21. A self-aligned method of forming a semiconductor memory array of floating gate memory cells in a semiconductor substrate, each memory cell having a floating gate, a first terminal, a second terminal with a channel region therebetween, and a control gate, the method comprising the steps of:

a) forming a plurality of spaced apart isolation regions on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions;

b) forming a plurality of spaced apart first trenches across the active regions and isolation regions which are substantially parallel to one another and extend in a second direction that is substantially perpendicular to the first direction, each of the first trenches being substantially rectangularly shaped, and forming a first layer of conductive material in each of the active regions adjacent to the first trenches and disposed over a first layer of insulation material;

c) forming a second layer of insulation material in each of the active regions that is disposed adjacent to and over the first layer of conductive material;

d) filling each of the first trenches with a second conductive material to form blocks of the second conductive material having a substantially rectangular shape, wherein for each of the active regions, each of the blocks is adjacent to the second layer of insulation material and is insulated from the substrate;

e) forming a sidewall spacer of a conductive material immediately adjacent to and contiguous with each of the blocks along the second direction, wherein for each active region each spacer is disposed over the second layer of insulation material and the first layer of conductive material;

f) forming a plurality of first terminals in the substrate, wherein in each of the active regions each of the first terminals is adjacent to one of the blocks; and

g) forming a plurality of second terminals in the substrate, wherein in each of the active regions each of the second terminals is spaced apart from the first terminals and is below the first layer of conductive material.

22. The method of claim 21, wherein the formation of the second layer of insulation material includes oxidizing top and side portions of the first layer of conductive material in each active region.

23. The method of claim 21, further comprising the steps of:

h) forming a plurality of spaced apart second trenches across the active regions and isolation regions which are substantially parallel to one another and extend in the second direction; each of the second trenches being formed between selected pairs of the blocks and extending through the first layer of conductive material and the first layer of insulation material to expose the second terminal;

i) forming a third layer of insulation material along sidewalls of the second trenches;

j) filling each of the second trenches with a conductive material that is insulated from the first conductive layer by the third layer of insulation material.

24. The method of claim 23, wherein the formation of the third layer of insulation material includes oxidizing end portions of the first layer of conductive material that face the second trenches.

25. The method of claim 23, wherein the formation of the third layer of insulation material includes forming a pair of inner sidewall spacers of an insulation material along sidewalls of each of the second trenches.

26. The method of claim 23, wherein the formation of the third layer of insulation material includes the steps of:

oxidizing end portions of the first layer of conductive material that face the second trenches; and

forming a pair of inner sidewall spacers of an insulation material along sidewalls of each of the second trenches.

27. The method of claim 21, wherein each of the blocks and corresponding spacer formed contiguously therewith form a control gate having a notch at the connection between the block and the spacer.

28. The method of claim 21, further comprising the step of forming a layer of metalized silicon on each of the blocks of second conductive material.

29. The method of claim 21, wherein the formation of the first trenches comprises the steps of:

forming at least one layer of material over the first layer of conductive material,

selectively etching through the at least one layer of material to form top portions of the first trenches;

forming a pair of sidewall spacers on side walls of each of the first trenches;

etching between each pair of the sidewall spacers of each of the first trenches and through the first layer of conductive material to form bottom portions of the first trenches;

wherein the bottom portions of the first trenches have a smaller width than that of the top portions of the first trenches.

30. The method of claim 21, wherein at least a portion of the second layer of insulation material is formed by forming a layer of insulation material along entire sidewalls of the first trenches.

31. The method of claim 21, wherein at least part of the second layer of insulation material is formed by forming a layer of insulation material on an upper surface of the first layer of conductive material.

32. The method of claim 21, wherein:

the formation of the first trenches includes the formation of intermediate trenches between selected pairs of the first trenches across the active regions and isolation regions, the intermediate trenches are substantially parallel to one another and extend in the second direction; and

the filling of the first trenches includes the filling of the intermediate trenches with the second conductive material to form blocks of the second conductive material in the intermediate trenches.

33. The method of claim 32, further comprising the step of forming a layer of metalized silicon on each of the blocks of second conductive material.

34. The method of claim 32, further comprising the steps of:

h) forming a plurality of spaced apart second trenches across the active regions and isolation regions which are substantially parallel to one another and extend in the second direction, the second trenches being formed by removing the second conductive material in the intermediate trenches, and extending the intermediate trenches through the first layer of conductive material and the first layer of insulation material to expose the second terminal;

i) forming a third layer of insulation material along sidewalls of the second trenches;

j) filling each of the second trenches with a conductive material that is insulated from the first conductive layer by the third layer of insulation material.

35. The method of claim 21, further comprising the steps of:

forming a second sidewall spacer of insulating material along a sidewall of each of the blocks of conductive material; and

forming a layer of metalized silicon on each of the first terminals immediately adjacent to one of the second sidewall spacers, wherein each of the layers of metalized silicon is self-aligned to the one of the second sidewall spacers.

36. The method of claim 21, further comprising the step of:

forming a layer of metalized silicon on each of the blocks of second conductive material, wherein for each of the first trenches, a sidewall of the first trench aligns an edge of the metalized silicon to an edge of the block of second conductive material.

37. The method of claim 21, further comprising the step of:

forming a third layer of insulation material over the layer of metalized silicon, wherein for each of the first trenches, a sidewall of the first trench aligns an edge of the third layer of insulation material to an edge of the block of second conductive material.

38. The method of claim 35, further comprising the step of:

forming a conductive material over each of the layers of metalized silicon and up against the second sidewall spacer self aligned thereto.

39. The method of claim 35, wherein the formation of each of the second sidewall spacers includes forming a layer of insulation material between the second sidewall spacer and the sidewall of the block of conductive material.

40. The method of claim 21, further comprising the steps of:

forming a second sidewall spacer of insulating material along a sidewall of each of the blocks of conductive material such that pairs of the second sidewall spacers are adjacent to but spaced apart from each other with one of the first terminals substantially therebetween;

forming a layer of metalized silicon on each one of the first terminals between a pair of the second sidewall spacers corresponding to the one first terminal such the layer of metalized silicon is self-aligned to the one first terminal by the corresponding pair of second sidewall spacers;

forming a layer of passivation material over the active regions;

forming contact openings through the passivation material, wherein for each of the contact openings:

the contact opening extends down to and exposes one of the metalized silicon layers,

the contact opening has a lower portion bounded by the corresponding pair of second sidewall spacers, and

the contact opening has an upper portion that is wider than a spacing between the corresponding pair of second sidewall spacers; and

filling each of the contact openings with a conductive material.

41. An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

first and second spaced-apart terminals in the substrate of a second conductivity type, with a channel region therebetween;

a first insulation layer disposed over said substrate;

an electrically conductive floating gate disposed over said first insulation layer and extending over a portion of said channel region and over a portion of the second terminal;

a second insulation layer disposed over and adjacent the floating gate and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and

an electrically conductive control gate having a first portion and a second portion, the first portion being substantially rectangularly shaped and positioned immediately adjacent to the second insulation layer, the second portion being substantially a spacer connected to the first portion and disposed over the floating gate and insulated therefrom.

42. The device of claim 41, wherein the control gate forms a notch at the connection between the first portion and the second portion.

43. An array of electrically programmable and erasable memory devices comprising:

a substrate of semiconductor material of a first conductivity type;

spaced apart isolation regions formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions;

each of the active regions including a column of memory cells extending in the first direction, each of the memory cells including:

first and second spaced-apart terminals formed in the substrate having a second conductivity type, with a channel region formed in the substrate therebetween,

a first insulation layer disposed over said substrate including over said channel region,

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an electrically conductive floating gate disposed over said first insulation layer and extending over a portion of said channel region and over a portion of the second terminal, and

a second insulation layer disposed over and adjacent the floating gate and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and

a plurality of electrically conductive control gates each extending across the active regions and isolation regions in a second direction substantially perpendicular to the first direction and having a first portion that is substantially rectangular in shape and a second portion that is connected to the first portion and is substantially a spacer, wherein each of the control gates intercepts one of the memory cells in each of the active regions such that the first portion is positioned immediately adjacent to the second insulation layer therein and the second portion is disposed over the floating gate and insulated therefrom.

44. The device of claim 43, wherein the control gate forms a notch at the connection between the first portion and the second portion.

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45. A self-aligned method of forming a semiconductor memory array of floating gate memory cells in a semiconductor substrate, each memory cell having a floating gate, a first terminal, a second terminal with a channel region therebetween, and a control gate, the method comprising the steps of:

a) forming a plurality of spaced apart isolation regions on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions, the active regions each comprising a first layer of insulation material on the semiconductor substrate and a first layer of conductive material on the first layer of insulation material;

b) forming a plurality of spaced apart first trenches across the active regions and isolation regions which are substantially parallel to one another and extend in a second direction that is substantially perpendicular to the first direction; each of the first trenches exposing the first layer of the conductive material in each of the active regions;

c) forming a second layer of insulation material in each of the active regions that is disposed adjacent to and over the first layer of conductive material;

d) filling each of the first trenches with a second conductive material to form blocks of the second conductive material each having a substantially planar sidewall portion, wherein for each of the active regions, each of the blocks is adjacent to the second layer of insulation material and is insulated from the substrate;

e) forming a sidewall spacer of a conductive material immediately adjacent to and contiguous with each of the substantially planar sidewall portions along the second direction, wherein for each active region each spacer is disposed over the second layer of insulation material and the first layer of conductive material;

f) forming a plurality of first terminals in the substrate, wherein in each of the active regions each of the first terminals is adjacent to one of the blocks; and

g) forming a plurality of second terminals in the substrate, wherein in each of the active regions each of the second terminals is spaced apart from the first terminals and is below the first layer of conductive material.

46. The method of claim 45, wherein the formation of the second layer of insulation material includes oxidizing top and side portions of the first layer of conductive material in each active region.

47. The method of claim 45, further comprising the steps of:

h) forming a plurality of spaced apart second trenches across the active regions and isolation regions which are substantially parallel to one another and extend in the second direction; each of the second trenches being formed between selected pairs of the blocks and extending through the first layer of conductive material and the first layer of insulation material to expose the second terminal;

i) forming a third layer of insulation material along sidewalls of the second trenches;

j) filling each of the second trenches with a conductive material that is insulated from the first conductive layer by the third layer of insulation material.

48. The method of claim 47, wherein the formation of the third layer of insulation material includes oxidizing end portions of the first layer of conductive material that face the second trenches.

49. The method of claim 47, wherein the formation of the third layer of insulation material includes forming a pair of inner sidewall spacers of an insulation material along sidewalls of each of the second trenches.

50. The method of claim 47, wherein the formation of the third layer of insulation material includes the steps of:

oxidizing end portions of the first layer of conductive material that face the second trenches; and

forming a pair of inner sidewall spacers of an insulation material along sidewalls of each of the second trenches.

51. The method of claim 45, wherein each of the blocks and corresponding spacer formed contiguously therewith form a control gate having a notch at the connection between the block and the spacer.

52. The method of claim 45, further comprising the step of forming a layer of metalized silicon on each of the blocks of second conductive material.

53. The method of claim 45, wherein the formation of the first trenches comprises the steps of:

forming at least one layer of material over the first layer of conductive material,

selectively etching through the at least one layer of material to form top portions of the first trenches;

forming a pair of sidewall spacers on side walls of each of the first trenches;

etching between each pair of the sidewall spacers of each of the first trenches and through the first layer of conductive material to form bottom portions of the first trenches;

wherein the bottom portions of the first trenches have a smaller width than that of the top portions of the first trenches.

54. The method of claim 45, wherein at least a portion of the second layer of insulation material is formed by forming a layer of insulation material along entire sidewalls of the first trenches.

55. The method of claim 45, wherein at least part of the second layer of insulation material is formed by forming a layer of insulation material on an upper surface of the first layer of conductive material.

56. The method of claim 45, wherein:

the formation of the first trenches includes the formation of intermediate trenches between selected pairs of the first trenches across the active regions and isolation regions, the intermediate trenches are substantially parallel to one another and extend in the second direction; and

the filling of the first trenches includes the filling of the intermediate trenches with the second conductive material to form blocks of the second conductive material in the intermediate trenches.

57. The method of claim 56, further comprising the step of forming a layer of metalized silicon on each of the blocks of second conductive material.

58. The method of claim 56, further comprising the steps of:

h) forming a plurality of spaced apart second trenches across the active regions and isolation regions which are substantially parallel to one another and extend in the second direction, the second trenches being formed by removing the second conductive material in the intermediate trenches, and extending the intermediate trenches through the first layer of conductive material and the first layer of insulation material to expose the second terminal;

i) forming a third layer of insulation material along sidewalls of the second trenches;

j) filling each of the second trenches with a conductive material that is insulated from the first conductive layer by the third layer of insulation material.

59. The method of claim 45, further comprising the steps of:

forming a second sidewall spacer of insulating material along a sidewall of each of the blocks of conductive material; and

forming a layer of metalized silicon on each of the first terminals immediately adjacent to one of the second sidewall spacers, wherein each of the layers of metalized silicon is self-aligned to the one of the second sidewall spacers.

60. The method of claim 45, further comprising the step of:

forming a layer of metalized silicon on each of the blocks of second conductive material, wherein for each of the first trenches, a sidewall of the first trench aligns an edge of the metalized silicon to an edge of the block of second conductive material.

61. The method of claim 45, further comprising the step of:

forming a third layer of insulation material over the layer of metalized silicon, wherein for each of the first trenches, a sidewall of the first trench aligns an edge of the third layer of insulation material to an edge of the block of second conductive material.

62. The method of claim 59, further comprising the step of:

forming a conductive material over each of the layers of metalized silicon and up against the second sidewall spacer self aligned thereto.

63. The method of claim 59, wherein the formation of each of the second sidewall spacers includes forming a layer of insulation material between the second sidewall spacer and the sidewall of the block of conductive material.

64. The method of claim 45, further comprising the steps of:

forming a second sidewall spacer of insulating material along a sidewall of each of the blocks of conductive material such that pairs of the second sidewall spacers are adjacent to but spaced apart from each other with one of the first terminals substantially therebetween;

forming a layer of metalized silicon on each one of the first terminals between a pair of the second sidewall spacers corresponding to the one first terminal such the layer of metalized

silicon is self-aligned to the one first terminal by the corresponding pair of second sidewall spacers;

forming a layer of passivation material over the active regions;

forming contact openings through the passivation material, wherein for each of the contact openings:

the contact opening extends down to and exposes one of the metalized silicon layers,

the contact opening has a lower portion bounded by the corresponding pair of second sidewall spacers, and

the contact opening has an upper portion that is wider than a spacing between the corresponding pair of second sidewall spacers; and

filling each of the contact openings with a conductive material.

65. A self-aligned method of forming a semiconductor memory array of floating gate memory cells in a semiconductor substrate, each memory cell having a floating gate, a first terminal, a second terminal with a channel region therebetween, and a control gate, the method comprising the steps of:

a) forming a plurality of spaced apart isolation regions on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions;

b) forming a plurality of spaced apart first trenches across the active regions and isolation regions which are substantially parallel to one another and extend in a second direction that is substantially perpendicular to the first direction, and forming a first layer of conductive material in each of the active regions adjacent to the first trenches and disposed over a first layer of insulation material;

c) forming a second layer of insulation material in each of the active regions that is disposed adjacent to and over the first layer of conductive material;

d) filling each of the first trenches with a second conductive material to form blocks of the second conductive material each having a substantially planar sidewall portion, wherein for each of the active regions, each of the blocks is adjacent to the second layer of insulation material and is insulated from the substrate;

e) forming a sidewall spacer of a conductive material immediately adjacent to and contiguous with each of the substantially planar sidewall portions along the second direction, wherein for each active region each spacer is disposed over the second layer of insulation material and the first layer of conductive material;

f) forming a plurality of first terminals in the substrate, wherein in each of the active regions each of the first terminals is adjacent to one of the blocks; and

g) forming a plurality of second terminals in the substrate, wherein in each of the active regions each of the second terminals is spaced apart from the first terminals and is below the first layer of conductive material.

66. The method of claim 65, wherein the formation of the second layer of insulation material includes oxidizing top and side portions of the first layer of conductive material in each active region.

67. The method of claim 65, further comprising the steps of:

h) forming a plurality of spaced apart second trenches across the active regions and isolation regions which are substantially parallel to one another and extend in the second direction; each of the second trenches being formed between selected pairs of the blocks and extending through the first layer of conductive material and the first layer of insulation material to expose the second terminal;

i) forming a third layer of insulation material along sidewalls of the second trenches;

j) filling each of the second trenches with a conductive material that is insulated from the first conductive layer by the third layer of insulation material.

68. The method of claim 67, wherein the formation of the third layer of insulation material includes oxidizing end portions of the first layer of conductive material that face the second trenches.

69. The method of claim 67, wherein the formation of the third layer of insulation material includes forming a pair of inner sidewall spacers of an insulation material along sidewalls of each of the second trenches.

70. The method of claim 67, wherein the formation of the third layer of insulation material includes the steps of:

oxidizing end portions of the first layer of conductive material that face the second trenches; and

forming a pair of inner sidewall spacers of an insulation material along sidewalls of each of the second trenches.

71. The method of claim 65, wherein each of the blocks and corresponding spacer formed contiguously therewith form a control gate having a notch at the connection between the block and the spacer.

72. The method of claim 65, further comprising the step of forming a layer of metalized silicon on each of the blocks of second conductive material.

73. The method of claim 65, wherein the formation of the first trenches comprises the steps of:

forming at least one layer of material over the first layer of conductive material,

selectively etching through the at least one layer of material to form top portions of the first trenches;

forming a pair of sidewall spacers on side walls of each of the first trenches;

etching between each pair of the sidewall spacers of each of the first trenches and through the first layer of conductive material to form bottom portions of the first trenches;

wherein the bottom portions of the first trenches have a smaller width than that of the top portions of the first trenches.

74. The method of claim 65, wherein at least a portion of the second layer of insulation material is formed by forming a layer of insulation material along entire sidewalls of the first trenches.

75. The method of claim 65, wherein at least part of the second layer of insulation material is formed by forming a layer of insulation material on an upper surface of the first layer of conductive material.

76. The method of claim 65, wherein:

the formation of the first trenches includes the formation of intermediate trenches between selected pairs of the first trenches across the active regions and isolation regions, the intermediate trenches are substantially parallel to one another and extend in the second direction; and

the filling of the first trenches includes the filling of the intermediate trenches with the second conductive material to form blocks of the second conductive material in the intermediate trenches.

77. The method of claim 76, further comprising the step of forming a layer of metalized silicon on each of the blocks of second conductive material.

78. The method of claim 76, further comprising the steps of:

h) forming a plurality of spaced apart second trenches across the active regions and isolation regions which are substantially parallel to one another and extend in the second direction, the second trenches being formed by removing the second conductive material in the intermediate trenches, and extending the intermediate trenches through the first layer of conductive material and the first layer of insulation material to expose the second terminal;

i) forming a third layer of insulation material along sidewalls of the second trenches;

j) filling each of the second trenches with a conductive material that is insulated from the first conductive layer by the third layer of insulation material.

79. The method of claim 65, further comprising the steps of:

forming a second sidewall spacer of insulating material along a sidewall of each of the blocks of conductive material; and

forming a layer of metalized silicon on each of the first terminals immediately adjacent to one of the second sidewall spacers, wherein each of the layers of metalized silicon is self-aligned to the one of the second sidewall spacers.

80. The method of claim 65, further comprising the step of:

forming a layer of metalized silicon on each of the blocks of second conductive material, wherein for each of the first trenches, a sidewall of the first trench aligns an edge of the metalized silicon to an edge of the block of second conductive material.

81. The method of claim 65, further comprising the step of:

forming a third layer of insulation material over the layer of metalized silicon, wherein for each of the first trenches, a sidewall of the first trench aligns an edge of the third layer of insulation material to an edge of the block of second conductive material.

82. The method of claim 79, further comprising the step of:

forming a conductive material over each of the layers of metalized silicon and up against the second sidewall spacer self aligned thereto.

83. The method of claim 79, wherein the formation of each of the second sidewall spacers includes forming a layer of insulation material between the second sidewall spacer and the sidewall of the block of conductive material.

84. The method of claim 65, further comprising the steps of:

forming a second sidewall spacer of insulating material along a sidewall of each of the blocks of conductive material such that pairs of the second sidewall spacers are adjacent to but spaced apart from each other with one of the first terminals substantially therebetween;

forming a layer of metalized silicon on each one of the first terminals between a pair of the second sidewall spacers corresponding to the one first terminal such the layer of metalized silicon is self-aligned to the one first terminal by the corresponding pair of second sidewall spacers;

forming a layer of passivation material over the active regions;

forming contact openings through the passivation material, wherein for each of the contact openings:

the contact opening extends down to and exposes one of the metalized silicon layers,

the contact opening has a lower portion bounded by the corresponding pair of second sidewall spacers, and

the contact opening has an upper portion that is wider than a spacing between the corresponding pair of second sidewall spacers; and

filling each of the contact openings with a conductive material.

85. An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

first and second spaced-apart terminals in the substrate of a second conductivity type, with a channel region therebetween;

a first insulation layer disposed over said substrate;

an electrically conductive floating gate disposed over said first insulation layer and extending over a portion of said channel region and over a portion of the second terminal;

a second insulation layer disposed over and adjacent the floating gate and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and

an electrically conductive control gate having a first portion and a second portion, the first portion having a substantially planar sidewall portion and is positioned immediately adjacent to the second insulation layer, the second portion being substantially a spacer connected to the substantially planar sidewall portion and disposed over the floating gate and insulated therefrom.

86. The device of claim 85, wherein the control gate forms a notch at the connection between the first portion and the second portion.

87. An array of electrically programmable and erasable memory devices comprising:

a substrate of semiconductor material of a first conductivity type;

spaced apart isolation regions formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions;

each of the active regions including a column of memory cells extending in the first direction, each of the memory cells including:

first and second spaced-apart terminals formed in the substrate having a second conductivity type, with a channel region formed in the substrate therebetween,

a first insulation layer disposed over said substrate including over said channel region,

an electrically conductive floating gate disposed over said first insulation layer and extending over a portion of said channel region and over a portion of the second terminal, and

a second insulation layer disposed over and adjacent the floating gate and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and

a plurality of electrically conductive control gates each extending across the active regions and isolation regions in a second direction substantially perpendicular to the first direction and having a first portion that has a substantially planar sidewall portion and a second portion that is connected to the substantially planar sidewall portion and is substantially a spacer, wherein each of the control gates intercepts one of the memory cells in each of the active regions such that the first portion is positioned immediately adjacent to the second insulation layer therein and the second portion is disposed over the floating gate and insulated therefrom.

88. The device of claim 87, wherein the control gate forms a notch at the connection between the first portion and the second portion.